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09/808,325

DATE: Friday, August 06, 2004

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		DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=ADJ	
☐	L7	L6 AND SIMULAT$3 SAME (pseudo OR random$7) SAME (vector OR PATTERN) SAME (DISCARD$3 OR remov$3)	1
☐	L6	(714/741,738, 739 OR 703/13,14,15,16,17,18,19,20,21,22).CCLS.	2589
☐	L5	('NN73033038')!.PN.	0
☐	L4	('20020133776')!.PN.	2
☐	L3	(DEFECT$3 OR ERR$7 OR FAIL$3 OR fault) SAME ((ic or (integrat$3 near2 circuit$3) or semi$1conduct$7 or semi conduct$7 or memor$7 or stor$4 or array or chip or die or dice) OR integrated NEAR2 (digital OR circuit)) SAME SIMULAT$3 SAME (pseudo OR random$7) SAME (vector OR PATTERN) SAME (DISCARD$3 OR remov$3)	21
☐	L2	L1 AND (DEFECT$3 OR ERR$7 OR FAIL$3 OR fault) SAME integrated NEAR2 (digital OR circuit) SAME SIMULAT$3 SAME (pseudo OR random$7) SAME (vector OR PATTERN) SAME (DISCARD$3 OR remov$3)	3
☐	L1	integrated NEAR2 (digital OR circuit) SAME SIMULAT$3 SAME (pseudo OR random$7) SAME (vector OR PATTERN) SAME (DISCARD$3 OR remov$3)	3

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L2: Entry 3 of 3 File: TDBD Mar 1, 1973

DOCUMENT-IDENTIFIER: NN73033038
TITLE: Random DC Functional Test Pattern Discriminator. March 1973.

Disclosure Text (1):
3p. This is a technique for minimizing a random DC functional test pattern without software simulation for logic chip testing. - Refer to Fig. 1 for a random DC functional test pattern provided at the primary input of the logic chip, including three primary NAND logic blocks. The test pattern is in terms of logic 1's and 0's. Between any two adjacent patterns, there is only one input change (either a logic 1 or 0). By comparing the particular pattern (n) with its immediate predecessor (number n-1), the single input change may be located. These changes in each pattern have been enclosed in a square in the Fig. 1 illustration. From a given digitized logic chip description, it is easy to sort out the chip's primary inputs and their immediate connected logic blocks in the chip. A block is qualified as a primary logic block when all its inputs serve as primary inputs to the chip. Thus, each of the blocks shown in Fig. 1 are primary logic blocks. Once the single input change between two adjacent test patterns is located, the affected primary logic block(s) may be traced out from the list of primary logic blocks vs. primary inputs. - In DC stuck-fault theory, it is not desirable to have patterns to any one NAND block with two or more logic 0 inputs. Patterns of good quality should only consist of one logic 0 per input per pattern, and one additional pattern with logic 1's for all inputs. For a NAND circuit with two or more inputs, if the previous pattern (n-1) had a logic 0 input, and if the single input change in the present pattern (n) provided two or more logic 0's, then the present pattern will not cause any significant difference from the previous one. Hence, the present pattern is redundant and may be eliminated without effecting pattern sequence. - Similarly, if the previous pattern had two or more logic 0 inputs on a NAND primary block, and the single input change in the present pattern created one less logic 0 at the same logic block, then the previous pattern may be eliminated due to redundancy. It is so chosen because the pattern with the fewer logic 0 inputs is more likely to change into a meaningful pattern later. If the change from one test pattern to the next results in an input change to a pattern which effects two or more primary logic blocks, and if the predicted output of one of the affected primary blocks is to be changed due to the potential minimization, then the pattern is preserved. An example is shown in Fig. 3. - As circuit density increases in large-scale integrated circuit chips, the chances of having logic blocks with two or more inputs is much greater than single input blocks as primary circuit blocks. If it is assumed that all inputs have equal chances of having two or more 0 inputs occur at a HAND block, then for a two input block, chances are one in every four patterns, for a three input block it is four in eight patterns, while in a four input block it would be eleven in sixteen patterns. Although these figures are not precise because of the random nature of the test pattern, it gives a good indication of the increased time savings as the chances for two or more 0's grows in proportion to the number of inputs to a primary input block. Because of the duality between NAND and NOR circuits, everything stated for NAND circuits is equally applicable to NOR circuits by substituting logic 0's for logic 1's. - As illustrated in Fig. 1, the patterns one through eleven were previously applied to the logic chip in sequence. By the present method, these patterns are examined sequentially starting at pattern 1. Going from pattern 1 to 2 a single input change is found to effect NAND block 3

only. Since both patterns have two or more 0 inputs on block 3, pattern 1 is eliminated as a nonessential pattern. This is because pattern 2 has fewer 0 inputs and is more likely to change into a good pattern later. Examining pattern 3 with respect to 2, the single input change still only affects logic block 3, pattern 2 is therefore eliminated because it has two 0 inputs on logic block 3. The elimination of patterns 1 and 2 did not create any output change from logic block 3, nor the chip, nor the sequence, and these two patterns were therefore expendable. - In accordance with the foregoing rules, patterns 3 and 4 remain as part of the pattern because the single input change creates only a single logic signal input on logic blocks 3 and 1, respectively. Pattern 5 is eliminated due to the double 0 inputs on logic block 1, and it essentially makes no output change at logic block 1 with respect to pattern 4. Pattern 6 is eliminated when it is compared with pattern 7, because the only difference between them is the inputs to logic block 1. Pattern 7 only contains one 0 input and is therefore retained as a good pattern. Pattern 8 is removed because two 0's are created as input to logic block 2, and this pattern makes no change as compared with pattern 7. Pattern 9 contains three 0 inputs to logic block 2 and is therefore eliminated. Similarly, pattern 10 is eliminated. The single input change on pattern 11 creates only a single 0 input to logic block 2 and is therefore retained. - Fig. 2 illustrates the reduced patterns showing that the retention of patterns 3, 4, 7 and 11 now becomes patterns 1, 2, 3 and 4. Accordingly, eleven patterns are reduced to four without a reduction in the degree the circuit is exercised. Occasionally, it is possible to further reduce the new list of patterns by removing the patterns that become redundant, due to the fact that in the new arrangement they are adjacent to each other. This minimization of random DC functional test patterns is accomplished without software simulation for logic chip testing.

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